SECOND-HARMONIC REFLECTOR TYPE HIGH-GAIN FET FREQUENCY DOUBLER OPERATING IN K-BAND

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ABSTRACT

High gain FET frequency doubler with second harmonic reflector in input circuit has been developed. The reflector position which gives maximum multiplication gain depends on line loss. The relation between multiplication gain and the reflector position is varying with line loss.

K-band frequency doubler designed by this theory was fabricated. Good coincidence was obtained with high gain of 6dB.

INTRODUCTION

A RF local source with excellent frequency stability and very low phase noise is required in communication fields. Such source is obtained by using multipliers and crystal oscillators. Though diodes or FETs are used for multipliers,FETs are more profitable because of high gain and suitability to MMICs(1). So we deal with a FET multiplier.

Rauscher gave the design method of the second harmonic reflector type FET frequency doubler(2).In this design method,transmission line is restricted to be lossless. But we found that the reflector position which gives the maximum multiplication gain depend on line loss. Here,we will present the design considerations and results for the FET doubler.

A K-band FET doubler which was designed by this theory has been fabricated . The multiplication gain of 6dB is obtained.

DESIGN

Fig.1 shows the block diagram of the second harmonic reflector type FET frequency doubler. The matching circuit for fundamental frequency(f0) wave and the reflector for second harmonic(2f0) wave are placed at the input ,and the matching circuit for 2f0 wave and the reflector for f0 wave at the output(3).

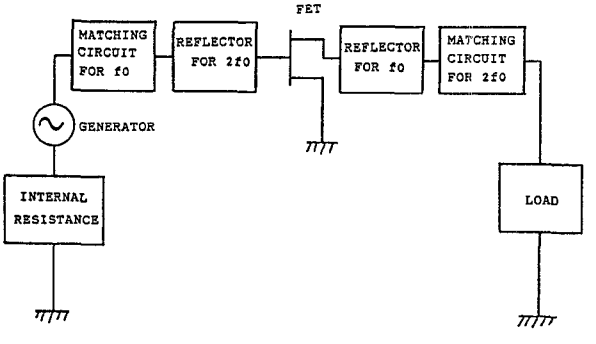

Fig.1 Block diagram of the second harmonic reflector type FET frequency doubler.

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Fig.2 shows the equivalent circuit of the FET frequency doubler shown in Fig.1.The open circuited stub with the electrical length $\pi/4$ is placed at electrical length θ_1 for f0 wave appart from the gate of the FET.

Second harmonic output power P2 in Fig.2 was calculated with harmonic balance method(4). Parameters of the FET in Fig.2 are given in Fig.3. Fig.4 shows the P2 Vs. θ_1 characteristics with the line loss parameter α at Vgs=-1V and Vds=3V. In this case, f0 is 9.75GHz and the input power Pin is -3dBm.

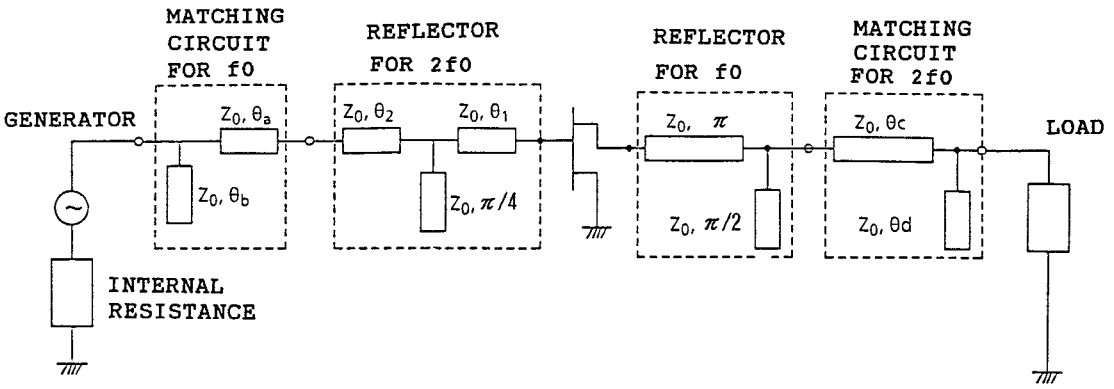
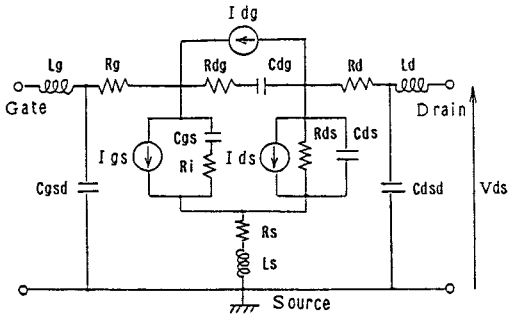
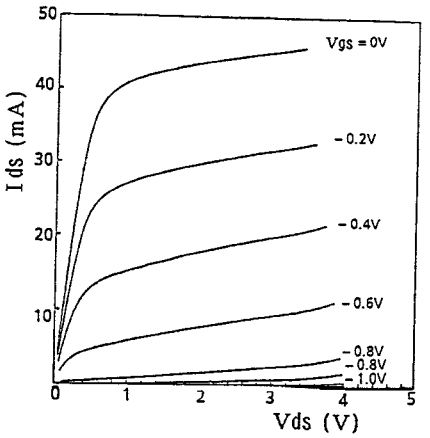


Fig.2 Equivalent circuit of the reflector type FET frequency doubler.



Lg	0.087	nH	Cdg	0.062	pF	Ls	0.032	nH
Cgsd	0.008	pF	Rdg	0.115	Ω	Rd	0.053	Ω
Rg	2.033	Ω	Cds	0.055	pF	Cdsd	0.036	pF
Cgs	0.165	pF	Rds	913.91	Ω	Ld	0.111	nH
Ri	1.282	Ω	Rs	1.498	Ω			

(a)



(b)

Fig.3 (a)Equivalent circuit model and (b)Ids vs.Vds characteristics for the FET used in this calculation.

It is seen from Fig 4 that the output power P2 is dependent on θ_1 and α. In the case of lossless line, maximum values of P2 appear periodically at the $\pi/2$ interval of θ_1, but in the lossy line, the lower maximum values of P2 appear periodically at interval π of θ_1. According to computer simulation, gate voltage at lower maximum values of P2 is found to be very lower, and so the input circuit is considered to be the circuit at series resonance with low external Q for f0 wave, which is not observed in lossless line.

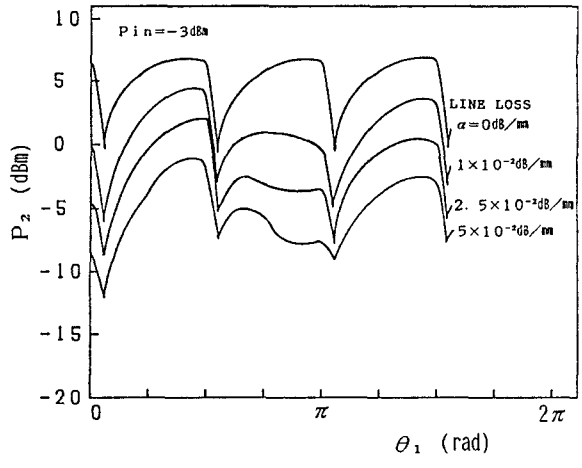


Fig.4 Calculated P2 vs. θ_1 characteristics as the line loss α is parameter.

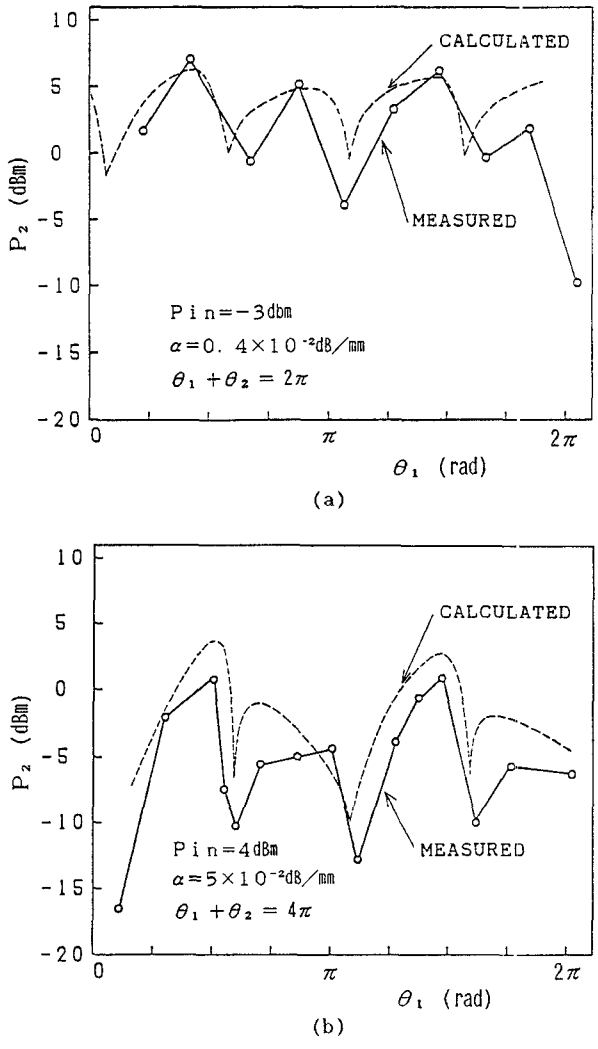


Fig.5 P2 vs. θ_1 characteristics for (a) low loss line, (b) high loss line.

This theory was verified with experimental model. The results are shown in Fig.5(a), (b), with experimental values by solid line and calculated values by dotted line. Fig.5(a) is for low loss line($\alpha=0.4\times10^{-2}$dB/mm), (b) for high loss line ($\alpha=5\times10^{-2}$dB/mm), f0=9.75GHz. Good coincidence was obtained.

FET DOUBLER MODULE

Fig.6 shows the photograph of the FET doubler module designed at 24GHz band. A FET doubler and a buffer amplifier are packaged in this module. For the miniaturization of the module, thin substrate is used, and so transmission line loss can not be neglected. Therefore, to obtain the maximum P2, the reflector position of 2f0 is determined by the above mentioned theory.

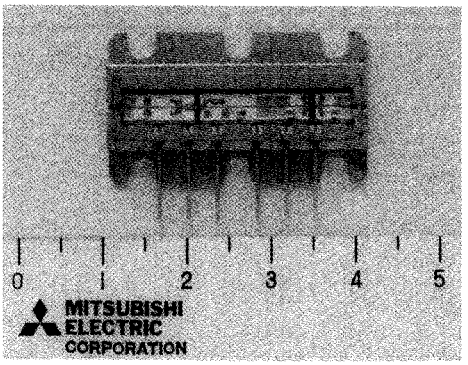


Fig.6 FET doubler module designed at 24GHz band.

Fig.7 shows the P2 vs.Pin characteristics at the center frequency. The multiplication gain of the FET doubler 6dB is achieved when the input power is -3dBm. Fig.8 shows a frequency dependence of output power with 7dBm input power.

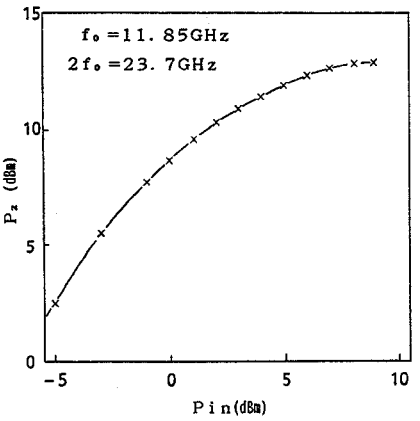


Fig.7 Pin vs.P2 characterisstics at the center frequency.

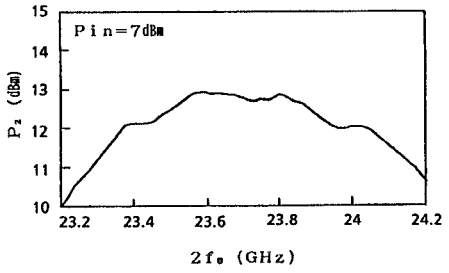


Fig.8 Frequency dependence of output power for +7dBm input.

CONCLUSION

Second harmonic reflector type high gain FET frequency doubler operating at K-band which has been developed in Mitsubishi Electric Corporation was described. In the design,line loss was taken into consideration and the position of the second harmonic reflector was determined according to the theory. Multiplication gain 6dB was obtained with the fablicated module.

REFERENCES

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